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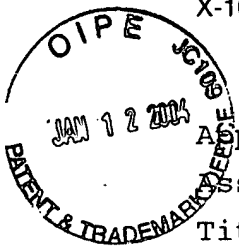
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application / Conf. No.	10/075,178 / 7288
	Filing Date	February 14, 2002
	First Named Inventor	Andy H. Gan
	Examiner Name	Binh C. Tat
	Art Unit	2825
	Patent No.	
Mail Stop: NON-FEE AMENDMENT	Attorney Docket Number	X-1068 US
Express Mail Receipt No.		
Total Number of Pages in This Submission		

ENCLOSURES (check all that apply)		
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<input type="checkbox"/> Preliminary Amendment	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Customer Number	24309 (Customer Number)	Reg. Number 51,959
Attn: Justin Liu		
Signature		
Date	January 9, 2004	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on this date: January 9, 2004			
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This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

IN THE UNITED STATES PATENT OFFICE

Applicant: Andy H. Gan
Assignee: Xilinx, Inc.
Title: "Method and Apparatus for Routing Interconnects to
Devices with Dissimilar Pitches"

Serial No.: 10/075,178 File Date: February 14, 2002
Examiner: Binh C. Tat Art Unit: 2825
Docket No.: X-1068 US Conf. No.: 7288

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

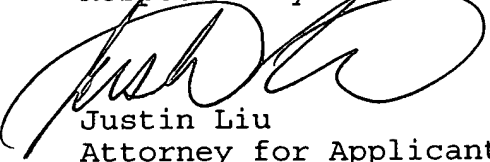
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner One Hundred (100) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. The enclosed references are being cited after the receipt of a first office action but prior to any final action.

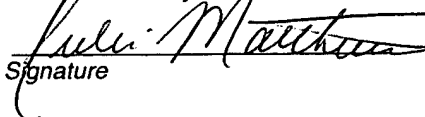
Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,


Justin Liu
Attorney for Applicant
Reg. No. 51,959

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(use as many sheets as necessary)

Sheet	1	of	7
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Complete if Known

Application / C. nf. No.	10/075,178 / 7288
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Art Unit	2825
Examiner Name	Binh C. Tat
Attorney Docket Number	X-1068 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
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		US- 5,347,181	09-13-94	Ashby et al.	
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		US- 5,552,722	09-03-96	Kean	
		US- 5,914,616	06-22-99	Young et al.	
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		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		Country Code ² -Number⁴ -Kind Code ³ (if known)				
		EP 0315275 A2	10-05-89	LSI Logic		
		WO 93 25968 A1	12-23-93	Furtek		
		EP 0 905 906 A2	03-31-99	Lucent		
		EP 1 235 351 A1	08-28-02	Matsushita Electric		

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		Art Unit	2825		
		Examiner Name	Binh C. Tat		
Sheet	2	of	7	Attorney Docket Number	X-1068 US

OTHER -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		MICHAEL I. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

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Sheet	3	of	7
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Application / C nf. No.	10/075,178 / 7288
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		Number - Kind Code (if known)			
		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 6,483,342	11-19-02	Britton et al.	
		US- 6,026,481	02-15-00	New et al.	
		US- 5,705,938	01-06-98	Kean	
		US- 5,500,943	03-19-96	Ho et al.	
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		US- 5,809,517	09-15-98	Shimura	
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		US- 5,933,023	08-03-99	Young	
		US- 09/991,412	11-16-01	Herron et al.	
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		US- 5,874,834	02-23-99	New	
		US- 5,835,405	11-10-98	Tsui et al.	

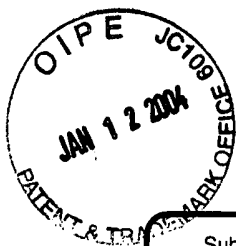
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OTHER -- NON PATENT LITERATURE DOCUMENTS

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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC, April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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OTHER -- NON PATENT LITERATURE DOCUMENTS			
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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch 3, pp 3-7 TO 3-17; 3-76 TO 3-87, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		XILINX, INC., "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	

Examiner Signature		Date Considered	
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		US- 6,519,753	02-11-03	Ang	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
		US- 6,539,508	03-25-03	Patrie et al.	
		US- 6,587,995	07-01-03	Duboc et al.	
		US- 6,242,945	06-05-01	New	
		US- 6,460,172	10-01-02	Insenser Farre et al.	
		US- 6,353,331	03-05-02	Shimanek	
		US- 6,507,942	01-14-03	Calderone et al.	
		US- 6,518,787	02-11-03	Allegrucci et al.	
		US- 6,522,167	02-18-03	Ansari et al.	
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